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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/029,679	12/21/2001	Gregg A. Bouchard	3-7-4-4-7-2	3296

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EXAMINER	
TRUONG, LAN DAI T	
ART UNIT	**PAPER NUMBER**
2143	

DATE MAILED: 12/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/029,679	BOUCHARD ET AL.	
	Examiner	Art Unit	
	Ian dai thi truong	2143	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21/21/01* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 05/22/03
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim rejections-35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1-2, 4, 10-11 are rejected under 35 U.S.C. 102(e) as being anticipated by Wallis (U.S. 4,149,243), "Wallis", herein after.

Regarding to claims 1, which is exemplary with claim 10-11:

Wallis discloses a system, which can be implemented in a computer hardware or software code for processing system, comprising:

First processing circuitry for performing a first function; at least second processing circuitry for performing a second function: (Wallis discloses a method for executing system supervisory and task management functions. Wallis teaches the control processor can initiate tasks to be perform by "a first subunit processor as Data Transfer Controller" which is equivalent to "first processing circuitry" for and "a second subunit processor as Arithmetic processor" which is equivalent to "second processing circuitry": abstract: lines 1-37; column 2, lines 1-52; column 3, lines 41-67; column 4, lines 1-7)

First memory circuitry, coupled to the first processing circuitry, for storing received packets, at least a portion of the packets stored by the first memory circuitry being usable by the

first processing circuitry in accordance with the first function; at least second memory circuitry, coupled to the second processing circuitry, for storing at least a portion of the same packets stored in the first memory circuitry, at least a portion of the packets stored in the second memory circuitry being usable by the second processing circuitry in accordance with the second function: (Wallis discloses the working stored has two storage banks, "left bank" which is equivalent to "first memory circuitry," and "right bank" which is equivalent to "second memory circuitry". And left bank stored new data which is load to the AP for processing, while the right bank is loading result data processed by the AP into the DTC for transmission to the bulk store, this process is shared functionality with "the second memory stores at least a portion of the same packets stored in the first memory circuitry": column 4, lines 30-40)

Regarding to claims 2, 4:

Wallis discloses a method as discuss in claim 1, which further includes wherein the first processing circuitry, the first memory circuitry, the second processing circuitry and the second memory circuitry are implemented on the same integrated circuit: (Wallis discloses a multiprocessor system" which is shared functionality with "a integrated circuit," therefrom, the first subunit processor implements first function, the second subunit processor implements second function. The subunit processor performed under controls of the other one within the multiprocessor system: column 2, lines 28-52)

Claim rejections-35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or descry
bed as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 15-16 and 18-20 are rejected under 35 U.S.C 103(a) as being un-patentable over Rostoket et al. (U.S. 5,623,494) in view of Wallis (U.S. 4,149,243), further in view of Aydemir et al. (U.S. 6,771,652)

Regarding to claims 15 and 18:

Storing the reassemble packet in a first memory, at least a portion of the reassemble packet stored by the first memory being usable by the first processor in accordance with a first function: (Rostoket discloses method of reassembling ATM cells and storing in each "host unit" which is exemplary with "a processor": abstract, lines 1-29)

However, Rostoket does not explicitly disclose wherein at least a portion of the subset of received packets reassemble by the first re-assembler may be reassembled in at least a second re-assembler for storage in at least a second memory usable by at least second processor in accordance with a second function

Wallis discloses the working stored has two storage banks, "left bank" which is equivalent to "first memory circuitry," and "right bank" which is equivalent to "second memory circuitry". And left bank stored new data which is load to the AP for processing, while the right

bank is loading result data processed by the AP into the DTC for transmission to the bulk store, this process is shared functionality with "the second memory stores at least a portion of the same packets stored in the first memory circuitry": column 4, lines 30-40

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Wallis's ideas of co-operation the processing of two separate processing with Rostoket's system in order to system in order to reduce processing delay, see (Wallis: column 1, lines 45-50)

However, Rostoket- Wallis does not explicitly discloses assembling subsets of received packets into reassembled packets in a first assembler

Aydemir discloses method of using reassembler to reassemble data packets: (column 1, lines 25-45)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Aydemir's ideas of co-operation the processing of two separate processing with Rostoket- Wallis's system in order to system in order to classify packet providing to the switch, see (Aydemir: column 1, lines 25-46)

Regarding to claims 16, 19:

In addition to rejection in claims 15 and 18, Wallis-Rostoket-Aydemir further discloses wherein the first processing circuitry, the first memory circuitry, the second processing circuitry and the second memory circuitry are implemented on the same integrated circuit: (Wallis discloses a multiprocessor system" which is shared functionality with "a integrated circuit," therefrom, the first subunit processor implements first function, the second subunit processor

implements second function. The subunit processor performed under controls of the other one within the multiprocessor system: column 2, lines 28-52)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Wallis's ideas of co-operation the processing of two separate processing with Rostoket's system in order to system in order to reduce processing delay, see (Wallis: column 1, lines 45-50)

Regarding to claim 20:

In addition to rejection in claim 18, Wallis-Rostoket-Aydemir further discloses wherein the first processor and the first memory are implemented on a first integrated circuit, and the second processor and the second memory are implemented on a second integrated circuit: (Wallis discloses a method for executing system supervisory and task management functions. Wallis teaches the control processor can initiate tasks to be perform by "a first subunit processor as Data Transfer Controller" which is equivalent to "first processing circuitry" for and "a second subunit processor as Arithmetic processor" which is equivalent to "second processing circuitry": abstract: lines 1-37; column 2, lines 1-52; column 3, lines 41-67; column 4, lines 1-7)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Wallis's ideas of co-operation the processing of two separate processing with Rostoket's system in order to system in order to reduce processing delay, see (Wallis: column 1, lines 45-50)

Claim 17 are rejected under 35 U.S.C 103(a) as being un-patentable over Wallis-Rostoket -Aydemir further in view of Van Ostrand et al. (U.S. 4,593,357)

Regarding to claim 17:

Wallis-Rostoket –Aydemir discloses the invention substantially as disclosed in claim 15, but does not explicitly teach wherein the first processing circuitry and the first memory circuitry are implemented on a first integrated circuit, and the second processing circuitry and the second memory circuitry are implemented on a second integrated circuit

However, Van Ostrand a plurality of integrated circuits are housed in separate circuit boards, see, (Van Ostrand: column 5, lines 18-19)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Van Ostrand ideas of housing a plurality of integrated circuits in separate circuit board with Wallis-Rostoket –Aydemir's's system in order to reduce processing delay, see (Wallis: column 1, lines 45-50)

Claim 6, 13-14 are rejected under 35 U.S.C 103(a) as being un-patentable over Wallis in view of Grow (U.S. 6,629,147)

Regarding to claims 6 and 13-14:

Wallis discloses the invention substantially as disclosed in claim 1, but does not explicitly teach wherein the first processing circuitry and the second processing circuitry operate between a packet network interface and a switch fabric of the packet switching device

Grow discloses switch used to assign and transmit signals into associated destination: (figure 1)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Grow's ideas of using switch to assign reassembled signals with Wallis's system in order to reduce process delay, see (Wallis: column 1, lines 45-50)

Claims 3, 5 are rejected under 35 U.S.C 103(a) as being un-patentable over Wallis in view of Van Ostrand et al. (U.S. 4,593,357)

Regarding to claims 3, 5:

Wallis discloses the invention substantially as disclosed in claims 1 and 15, but does not explicitly teach wherein the first processing circuitry and the first memory circuitry are implemented on a first integrated circuit, and the second processing circuitry and the second memory circuitry are implemented on a second integrated circuit

However, Van Ostrand a plurality of integrated circuits are housed in separate circuit boards, see (Van Ostrand: column 5, lines 18-19)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Van Ostrand's ideas of housing a plurality of integrated circuits in separate circuit board with Wallis's system in order to reduce process delay, see (Wallis: column 1, lines 45-50)

Claims 7-9 are rejected under 35 U.S.C 103(a) as being un-patentable over Wallis-Grow in view of Sethuram et al. (U.S. 6,058,114)

Regarding to claim 7:

Wallis- Grow discloses the invention substantially as disclosed in claim 6, but does not explicitly disclose wherein the first function comprises a packet classifying operation

However, Sethuram discloses "a sorter" which is shared functionality with "classifying": (abstract, lines 1-15)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Sethuram's ideas of housing a plurality of integrated circuits in

separate circuit board with Wallis- Grow's system in order to reduce process delay, see (Wallis: column 1, lines 45-50)

Claims 8-9 are rejected under 35 U.S.C 103(a) as being un-patentable over Wallis in view of Gemar et al. (U.S. 6,483,839)

Regarding to claims 8 and 9:

Wallis discloses the invention substantially as disclosed in claims 1, but does not explicitly discloses wherein the second processing circuitry and the second memory circuitry comprise a traffic manager

However, Gemar discloses a traffic manager: (abstract, lines 1-12)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Gemar's ideas of using the operation provide by traffic manager with Wallis's system in order to control network traffic, see (Gemar: abstract, lines 1-12)

Claims 12 is rejected under 35 U.S.C 103(a) as being un-patentable over Wallis in view of Rostoket et al. (U.S. 5,623,494)

Regarding to claim 12:

Wallis discloses the invention substantially as disclosed in claims 1, but does not explicitly wherein the packet subsets are cells

Rostoket discloses method of reassembling ATM cells: (abstract, lines 1-5)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Rostoket's ideas of using reassembling segmented cells with Wallis's system in order to transmitting reassemble signals into associated processor unit, see (Rostoket: abstract, lines 1-12)

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to lan dai thi truong whose telephone number is 571-272-7959. The examiner can normally be reached on monday- friday from 8:30am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Wiley can be reached on (571) 272-3923. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lan Dai Thi Truong
Examiner
Art Unit 2143

Ldt
12/08/2005

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